Low Power Dual Channel Broadband SFCW Generator

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Abstract: SFCW based high resolution RADAR is an alternative for broadband impulse based RADAR. Though the hardware for an impulse RADAR is simple, precise control of impulse shape and elimination of other artifacts such as jitter, ringing are difficult. Though SFCW technique does not have such problem but hardware complexity and power consumption prevents system designers from using SFCW techniques. Especially for a hand held device power consumption is of prime importance .A low power proto Broadband SFCW generator is designed and developed. The developed SFCW generator uses PLL with switched resonator VCO technology to achieve broadband SFCW .The SFCW generator uses sigma delta modulator and have precise phase control. The SFCW generator generates more than four octave wide bandwidth from 200MHz to 4GHz consuming only 1W of power .This SFCW generator is useful for heterodyne Receiver based SFCW RADAR.

The prototype waveform generator is subjected for impulse synthesize test and its performance is found satisfactory.

Key words: Step frequency continuous waveform (SFCW), Phase Locked Loop (PLL), Dwell Time, Frequency Hopping Time.

I INTRODUCTION

Broadband SFCW generator forms the heart of a typical high resolution RADAR. To achieve High Resolution we need to Generate Extremely High bandwidth. For example to achieve a resolution of 50mm we need to generate a bandwidth of 3GHz .Though the task of achieving higher resolution can be accomplished by transmitting a narrow pulse of the order of wanted time equivalent resolution ,maintaining the fidelity of pulse with sharp rise time and narrow width is extremely difficult though it seems to be trivial. In such cases synthesizing the narrow pulse by virtue of SFCW will mitigate the problem. However power consumption and compactness of the SFCW design is a compromise .This author has designed a SFCW generator which breaks the limit of power consumption and size factor .A description of a low power Dual channel SFCW Generator is presented .In addition to this SFCW generator has a very good flexibility in choosing the fundamental SFCW parameters like dwell time and frequency step. Dual channel can support heterodyne receiver architecture .The proposed method consists of

1. Two PLL each for one channel with internal VCO's
2. A low power Controller to control the PLL
3. Associated circuitry for amplification

II CONCEPTUAL DEISGN

The concept for this design is as follows. Use two PLL's to generate two channel of SFCW. The PLL will be continuously updated and should be synchronized to each other so that phase coherency referred back to the common reference is maintained between both the channel .The internal counter is operated in integer mode to remove phase ambiguity. Though fractional mode counting can give flexible count the instantaneous error accumulates as a growing phase error. Though this can be compensated in a perfect way by analog techniques, by current injection but it is not reliable over ageing and temperature effect. So the alternate way is to make a pseudo random pattern in the error due to fractional counting .If we use a sigma delta modulator output as a counter modulation signal then we can have more frequently occurring phase error and the spectrum corresponding to this will have a high pass profile .As VCO acts like an integrator ,along with the loop filter the high frequency noise is cleaned of in frequency domain which is equivalent to reducing the phase error in time domain. But this method requires extremely power full sigma delta modulator of atleast 20 bits and of order three or more to completely shave off the phase error. A 32 bit modulus will be ideal, but implementing a 32 bit sigma delta modulator will be a costly affair .So integer mode is chosen for the generation which has limitation in resolution of step size.

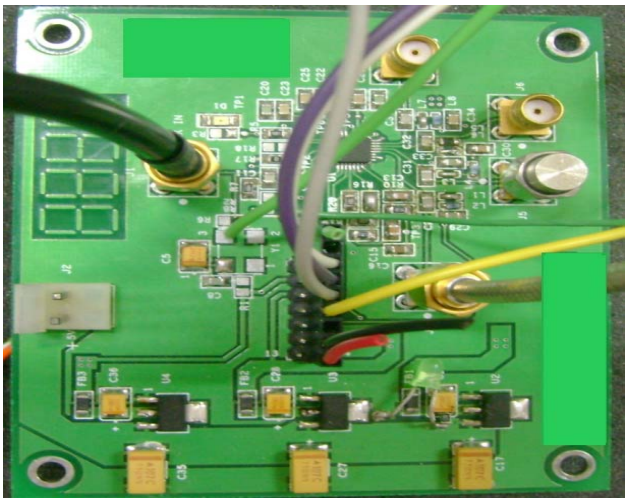


Figure1

III DESIGN APPROACH

For implementing low power and compact SFCW generator a PLL with integrated VCO is chosen, though this have a compromise in phase noise, but it is insignificant, The loop filter is designed to the tightest bandwidth of 20kHz to remove Phase noise .Though this has a impact on lock time the internal calibration time is a limiting factor in reducing

the lock time .The sensitivity of the VCO is around 23MHz .A third order type two loop filter is chosen for the PLL closed loop. The damping factor is chosen around 0.707, to avoid any oscillation without compromising the lock time .The charge pump current is around 1mA to get fast lock, which increases the loop gain .care should be taken while increasing the charge pump gain as it increases the loop gain takes the system to oscillation. Such oscillations are typical for a chargepump based Phase comparator .The reference frequency chosen is 26MHz which reduces the lock time .For a typical compact High resolution RADAR the Unambiguous range is 1 meter. The dual channels are configured with an offset of 13MHz .This offset will appear as IF frequency if the two channels are mixed in mixer .The RF output is muted during transient state saving the power off the system .In the typical implementation RF mute duty cycle of 50% is utilized which drastically reduces the power consumption .The input power supply of the system is 3.7V and the power supply voltage of all the active components are kept for 3.3V.This gives a power conversion efficiency of 89% as well as allow the usage of lithium ion battery to power up the system .

III IMPLEMENTATION

The implementation part consists of choosing a commercially available PLL along with a low power FPGA .Basically FLASH FPGA with low core voltage will consume less power .The main implementation logic is the Micro wire protocol which needs three wire to transfer the data .The serial clock of microwire should be same as that of PLL reference frequency .The internal counter should be loaded only during the rising edge of reference clock to ensure Phase coherency for all the spots to be generated

The reference clock of the two PLL should be sufficiently phase matched to avoid any Phase hit. To test the performance of Dual channel SFCW generator a Phase detector with high port to port isolation is implemented along with the setup. Figure shows the complete integrated setup.Figure1 shows the PLL board made out of FR4.

Figure 2

IV TEST RESULTS

The frequency transients of the SFCW generator is captured using Real time Spectrum Analyzer .Figure3 shows the captured results for a bandwidth of 110MHz .The mute till lock function is implemented and the results are verified to get 40dB isolation. The microwire interface is captured using logic analyzer and tested for its synchronization with the main clock. The fidelity of the waveform is confirmed through a subjective test of capturing the output of External Phase detector and taking IFFT in Matlab. Figure 4b confirms the quality of Dual channel SFCW. Figure 4a shows the Homodyne test results. As evident from the figure the homodyne system has self calibrating feature which reduces the spurious response in range domain of IFFT plot

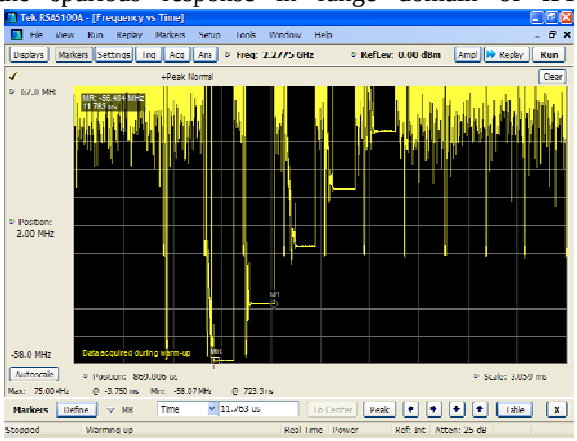
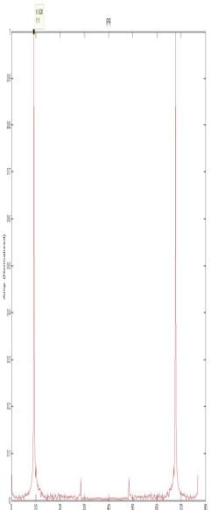


Figure3



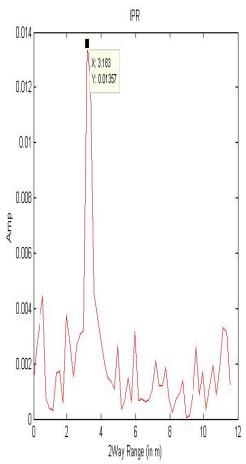


Figure 4a Figure 4b

V CONCLUSION AND FUTURE SCOPE

The current implementation is based on PLL with integer counter. The fractional spurious is preventing us from going for fractional mode of operation .But if we were able to make a 32 bit sigma delta modulator then the level of Phase

coherency can be taken to the level of an ideal text book SFCW performance

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Shri V AswinKumar started his career as RF designer with Electronics Research and Development Centre of India, Thiruvananthapuram in 2004.He was involved in the development of RF subsystems for countries first indigenous communication (TETRA) base-station .He joined DRDO in 2007 ,and since then worked for BJT ,LDMOS T/R module development, PLL-DDS based Synthesizers, Ultrabroadband Waveform generators and high performance Receivers. Currently he is working for High resolution RADARS. His field of interests are , MMIC design, LTCC design and Miniaturization of RF circuits

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